Abstract

[0042] A method for synthesizing a clock distribution system within an integrated circuit for compensating for clock skew within a global or top level clock distribution network begins with allocating at least one delaying circuit within each of functional circuits of the integrated circuit. An intra-functional clock distribution network is fabricated within each of the functional circuits. Once the intra-functional clock distribution network is fabricated, an inter-functional clock distribution network is constructed between each of the functional circuits. A clock skew for the inter-functional clock distribution network is determined. The clock skew is then compensated by inserting the delaying circuit at a terminal of the inter-function clock distribution network where each of the functional circuits is connected to the inter-functional clock distribution network.